We claim:

1	1. A mixed	analog/digital	integrated	circuit	comprising:
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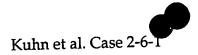
- (a) a silicon substrate having a surface,
- 3 (b) a digital device section in the substrate, the digital device section
- 4 comprising an array of MOS transistors operating at a voltage V_D that
- steps from a first value V_{D1} , to a second value V_{D2} ,
- 6 (c) a p-n junction guard ring surrounding the digital device section, the
- guard ring comprising impurity regions extending from the surface of the
- substrate to a depth of at least d below the surface of the substrate,
- 9 (d) an analog device section in the substrate spaced laterally from the
- digital device section, the analog device section comprising an array of
- MOS transistors operating with a voltage V_A that varies continuously
- 12 from V_{A1} to V_{A2} ,
- (e) a triple well isolation region comprising a doped layer that extends
- beneath the digital device region at a depth d and contacts the p-n
- junction guard ring,
- and wherein the analog device section is devoid of triple well isolation
- 17 region.
- 2. The integrated circuit of claim 1 wherein the array of MOS transistors in the
- 2 digital device section comprise pairs of CMOS transistors.

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- 3. The integrated circuit of claim 2 wherein the array of MOS transistors in the
- 2 analog device section comprise pairs of CMOS transistors.
- 4. The integrated circuit of claim 1 wherein d is in the range 2 10 microns.
- 5. An integrated circuit formed in a p-type silicon substrate and comprising:
- 2 (a) a digital device section, the digital device section having a first region,
- a second region and a third region and comprising:
- 4 (i) an n-well formed in the first region of the digital device section,
- 5 (ii) at least one p-channel transistor formed in the first n-well,
- $_{6}$ (iii) means for applying to the p-channel transistor a voltage $V_{\scriptscriptstyle D}$ that
- steps from a first value, V_{D1} , to a second value, V_{D2} ,
- (iv) at least one n-channel transistor formed in the second region of
- 9 the digital device section,
- (v) means for applying to the n-channel transistor a voltage V_D that
- steps from a first value, V_{D1} , to a second value, V_{D2} ,
- (vi) at least one n-well resistor formed in the third region of the
- 13 digital device section,
- (b) an analog device section, the analog section comprising a first region,
- and a second region, and comprising:
- (i) an n-well formed in the first region of the analog device section,
- (ii) at least one p-channel transistor formed in the first n-well,

18	(iii) means for applying to the p-channel transistor a voltage V_{A} that
19	varies over a range of voltages between a first value, V_{A1} , and a
20	second value, V_{A2} ,
21	(iv) at least one n-channel transistor formed in the second region of
22	the analog device section,
23	(v) means for applying to the n-channel transistor a voltage $V_{\mbox{\tiny A}}$ that
24	varies over a range of values between a first value, $V_{\rm Al}$, and a
25	second value, V_{A2} ,
26	(c) means for connecting the first and second regions of the digital device
27	section to digital V_{ss} ,
28 .	(d) means for connecting the first and second regions of the analog device
29	section, and the third region of the digital device section to analog $\ensuremath{V_{\text{SS}}}$,
30	(e) a first n-type guard ring surrounding the first, second, and third
31	regions of the digital device section, the first n-type guard ring extending
32	from the surface of the substrate to a depth of at least d below the surface
33	of the substrate,
34	(f) a second n-type guard ring surrounding the third region of the digital
35	device section, the second n-type guard ring situated within, and spaced
36	from, the first n-type guard ring and extending from the surface of the
37	substrate to a depth of at least d below the surface of the substrate,
38	(g) an n-type triple well isolation region selectively formed at a depth d
39	underneath said first and second regions of the digital device section and

joined to the first and second n-type guard rings.

- 6. The integrated circuit of claim 5 wherein d is in the range 2 10 microns.
- 7. An integrated circuit formed in an n-type silicon substrate and comprising: 1 (a) a digital device section, the digital device section having a first region, 2 a second region and a third region and comprising: 3 (i) a p-well formed in the first region of the digital device section, 4 (ii) at least one n-channel transistor formed in the first p-well, 5 (iii) means for applying to the n-channel transistor a voltage $V_{\scriptscriptstyle D}$ that 6 steps from a first value, $V_{\text{D1}}\text{, to a second value, }V_{\text{D2}}\text{ ,}$ 7 (iv) at least one p-channel transistor formed in the second region of 8. the digital device section, 9 (v) means for applying to the p-channel transistor a voltage V_D that 10 steps from a first value, $V_{\text{D1}}\text{, to a second value, }V_{\text{D2}}\text{ ,}$ 11 (vi) at least one p-well resistor formed in the third region of the 12 digital device section, 13 (b) an analog device section, the analog section comprising a first region, 14 and a second region, and comprising: 15 (i) a p-well formed in the first region of the analog device section, 16 (ii) at least one n-channel transistor formed in the first p-well, 17 (iii) means for applying to the n-channel transistor a voltage V_A that 18



19	varies over a range of voltages between a first value, V_{A1} , and a
20	second value, V _{A2} ,
21	(iv) at least one p-channel transistor formed in the second region of
22	the analog device section,
23	(v) means for applying to the p-channel transistor a voltage $V_{\rm A}$ that
24	varies over a range of values between a first value, V_{A1} , and a
25	second value, V_{A2} ,
26	(c) means for connecting the first and second regions of the digital device
27	section to digital V_{DD} ,
28	(d) means for connecting the first and second regions of the analog device
29 ·	section, and the third region of the digital device section to analog V_{DD} ,
30	(e) a first p-type guard ring surrounding the first, second, and third
31	regions of the digital device section, the first p-type guard ring extending
32	from the surface of the substrate to a depth of at least d below the surface
33	of the substrate,
34	(f) a second p-type guard ring surrounding the third region of the digital
35	device section, the second p-type guard ring situated within, and spaced
36	from, the first p-type guard ring and extending from the surface of the
37	substrate to a depth of at least d below the surface of the substrate,
38	(g) a p-type triple well isolation region selectively formed at a depth d
39	underneath said first and second regions of the digital device section and
40	joined to the first and second p-type guard rings.